## ABSTRACT OF THE DISCLOSURE

A TFT array substrate has a substrate with a pixel region and a switching region. A gate line has both a gate electrode that extends into the switching region and a gate pad is formed on the substrate. A gate pad electrode is formed on the gate pad. A data line includes both a source electrode that extends from the data line into the switching region and a data pad. A data pad electrode is formed on the data pad. A drain electrode that is spaced apart from the source electrode is over the gate electrode. A gate insulation layer covers the gate electrode and the substrate. Semiconductor layers, including a pure amorphous silicon layer and a doped amorphous silicon layer, and a protection layer extends over the source electrode, over the silicon layers, and over part of the drain electrode. A pixel electrode is formed on the pixel region. The pixel electrode contacts a side portion of the drain electrode. The TFT array substrate is fabricated using a back exposure.